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NICS

Case Study: Allinea Software Helps Scientists as They Port Code to New Architectures

Snapshot

Client: The Application Acceleration Center of Excellence (AACE), which sits within the Joint Institute for Computational Sciences (JICS), a shared institute of the University of Tennessee (UT) and the Oak Ridge National Laboratory (ORNL).

Challenge: As researchers port codes to new architectures such as the Intel® Xeon Phi™ coprocessors or GPGPU accelerators, complex changes can introduce software bugs.

Solution: Allinea DDT, a powerful tool that can debug applications on many Intel® Xeon Phi™ coprocessors and host processors simultaneously.

Results: A small error in scope that made a big difference in the results from a Boltzmann-BGK code is fixed in minutes.

Summary quote: "Squeezing the performance out of the newest architectures requires more in-depth understanding of code design, memory placement, and the complex relationships between different parallel coding paradigms than ever before. Allinea DDT is a tool that helps programmers and scientists like us dig down to the levels where print statements cannot reach." — Dr. Vincent C. Betro, Computational Scientist (NICS/JICS/ORNL)

In the race to adopt the newest supercomputing architectures, researchers need the best tools they can find. That's why developers at the Application Acceleration Center of Excellence are working with Allinea DDT.

The Beacon system at the Joint Institute for Computational Sciences at The University of Tennessee and Oak Ridge National Laboratory is a trailblazer of a new generation of systems using Intel® Xeon Phi™ coprocessor technology. To use this capability effectively, most software applications must be adapted to the hybrid architecture.

Developers at the Application Acceleration Center of Excellence (AACE) are leading the charge – combining multithreaded OpenMP constructs with parallel multi-process MPI functions in a number of key scientific software packages.

Weaving paradigms like OpenMP and MPI together can cause race conditions and other phenomena that are not easily debugged through print statements. With a handful of coprocessors, applications soon use thousands of cores and threads.

The AACE team has a new weapon in their armory. With Allinea DDT, developers can pinpoint failures quickly as it gives one view of every process in a parallel job, showing exactly what lines of code are being executed.

A Beacon for Green Computing

The Beacon system is not a Titan or Tianhe-2, but it did top the Green500 in November 2012 by computing at 2.499 GigaFLOP/Watt.

Even with those energy-conservation credentials, the high-performance system is not light on capability – employing 768 conventional cores and 11,520 accelerator cores to produce more than 210 TeraFLOP/s of combined computational performance. The system also provides 12 Terabytes of system memory, 1.5 Terabytes of coprocessor memory, and more than 73 Terabytes of SSD storage, in aggregate.

Each compute node is equipped with 2 Intel® Xeon® processors, 4 Intel® Xeon Phi™ coprocessors, 256 GB of RAM, and 960 GB of SSD storage.

"With hybrid architectures such as the Intel® Many Integrated Cores (MIC) architecture and GPGPU architectures, factors such as vector calculations, memory alignment, and multi-threading have become required to squeeze performance out of accelerators and make them the low-energy, high-compute power devices that will allow us to scale far into the 21st century," said Dr. Vincent Betro, Computational Scientist at AACE.

Unfortunately, these coding techniques are not always in the comfort zone of most scientists. So, when trying to port codes, issues often arise in the implementation of such techniques.

Developers soon find problems that cannot be debugged with print statements alone.

For instance, if multiple threads are running within multiple MPI ranks, the activity of the buffer and the order of

the print statements, even with good buffer-flushing practices, are non-deterministic between runs and often serve only to provide red herrings to researchers looking to find the real problem.

## Getting the Most from Boltzmann-BGK CFD

Kinetic approaches, such as the use of Boltzmann-BGK equations, are emerging as important methods for simulating challenging fluid flows in Computational Fluid Dynamics (CFD).

Researchers at AACE are developing a Boltzmann-BGK CFD solver for studying transitional fluid flows. To ensure correct behavior, the solver is verified throughout the development process against canonical test cases such as flow around airfoils.

As the initial solver evolved from serial, through MPI, and then to MPI + OpenMP, the Intel® Xeon Phi™ architecture was considered at each step of the design process. But as the development process continued and the team grew to several researchers and interns, bugs were introduced during the attempt to add sufficient fine-grained parallelism.

"Squeezing the performance out of the newest architectures requires more in-depth understanding of code design, memory placement, and the complex relationships between different parallel coding

This image shows a NACA 0012 airfoil at Mach 0.95 with a 1-degree angle of attack. Note the shock developing toward the tail on both the top and bottom surface of the wing.
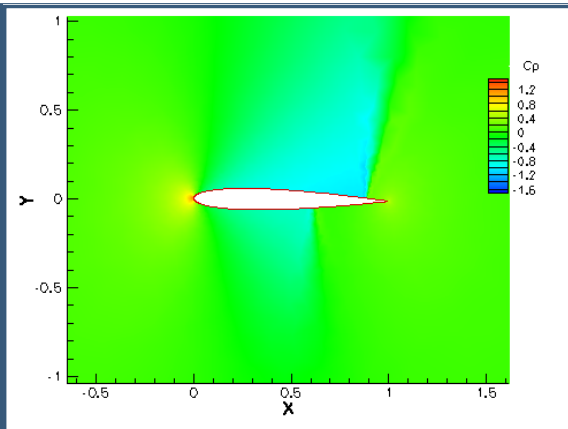
paradigms than ever before," said Betro.

"One intern struggled for six weeks to implement a Cartesian coordinate communicator construct. He initially was trying to figure out his issues with print statements. I showed him the debugger, and he rapidly determined where his error was and got a working model going again."

Allinea DDT to the Rescue

However, what did not become clear until later, when another researcher was running other test cases, was that we were getting physically incorrect results.

Incorrect results can lead to incorrect design decisions, and costly rectification later. Thus, being able to resolve software issues quickly is important, and that makes tools such as debuggers invaluable to CFD developers and researchers.

Using Allinea DDT running across both the Xeon host and the Xeon Phi coprocessor, Dr. Betro found

a loop that had been divided up into a first iteration version and a remaining iterations loop. A typo—of not removing a pair of curly braces—was causing variables that had been declared inside these braces to be out of scope elsewhere, thus yielding incorrect values.

"With the graphical Allinea DDT, I could see values of the variables on each MPI rank simultaneously—and in the threads—and determine that they were not changing as expected. By stepping through and seeing that the values were only correct on the first iteration in one area, I was soon able to diagnose and fix the problem."

"Allinea DDT can help programmers dig down to levels where non-deterministic print statements cannot reach."

With the results back to pre-porting levels of accuracy, development and further porting and optimization can continue, and Beacon can continue to shine more light on the hybrid future of high-performance computing.